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10/530,852	04/11/2005	Anthony Sanders		2280

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EXAMINER	
MCKIE, GINA M	

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2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/530,852	SANDERS ET AL.	
	Examiner	Art Unit	
	GINA MCKIE	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *082905*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because:

Figure 1 only contains numerical reference characters and fails to include corresponding word labels for easy identification of the figure elements.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because it contains legal phraseology. Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities:

The preliminary amendment to the specification requests replacing the paragraph that begins at page 4, line 22 with an amended paragraph. However, it is the paragraph that begins at page 4, line 29 that should be replaced with the aforementioned amended paragraph.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 17, 24, and 29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in

the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

According to claims 17, 24, and 29, a third clock generator circuit generates an extracted clock signal based on the average of a first phase difference (obtained from a first phase detector for detecting a phase difference between a rising edge of a periodic data signal and a rising edge of a rising edge clock signal) and a second phase difference (obtained from a second phase detector for detecting a phase difference between a falling edge of a periodic data signal and a falling edge of a falling edge clock signal) in a way that the probability distribution functions of the rising edges and falling edges of the data signal are individually averaged.

Interpreting the average of a phase difference in a phase locked loop, for example, in the sense of an arithmetic mean, the corresponding feature may be interpreted in at least two different ways:

- The arithmetic mean of a sequence of discrete samples of the first phase difference and the arithmetic mean of a sequence of discrete samples of the second phase difference are computed (i.e. averaging the differences separately). In this case both averages are zero, and it is consequently not possible to produce a meaningful clock signal based on these averages.
- The arithmetic mean of one discrete sample of the first phase difference and one discrete sample of the second phase difference is computed. If the transitions in the first loop are subject to a random jitter, then the detected first phase difference will be a random signal with zero mean (as indicated with the probability density function

(308) in Figure 3). Likewise, the detected second phase difference will be a random signal with zero mean. How to generate a clock signal based on two random signals which are devoid of any information remains entirely unclear.

To fill the teaching lacking in the claims with respect to the generation of the extracted clock signal, a person skilled in the art would consult to this end the written description and the drawings. The written description discloses in that respect on page 5 that the basic idea of the invention is to individually average the probability distribution functions of the rising and falling edges of the data signal using two independent phase locked loops. However, nothing is disclosed in the written description which would render it apparent to the skilled person how to compute these probability distribution functions based on the phase averages (which are either zero or a random signal with zero mean, as outlined above). Furthermore, the written description is completely silent about how the generation of the extracted clock signal results in the individual averaging of the probability distribution function. It is also pointed out that it is entirely unclear what the average of a probability distribution function might be, since it is an average in itself. Therefore, the description does not disclose the invention's essential features in sufficient detail to render it apparent to the skilled person how to put the invention into practice. The figures do not disclose any additional information with respect to the generation of the extracted clock signal, either.

To the argument that the phase difference of the phase locked loops in a transient or out-of-lock state may be useful in order to generate the extracted clock signal, it is noted that nothing to that respect is mentioned in the description about this

very complicated matter. To the person skilled in the art, it is by no means apparent how any useful information may be extracted from a transient state or an out-of-lock state of a PLL. The only other information provided by the description with respect to the generation of the extracted clock signal is that, in a further embodiment, the controller controls the generation of said clock signal so that the error rate of the extracted data is minimized (see, for example, the description on page 7, lines 5-8 or page 11, lines 1-2). This embodiment, however, also lacks the disclosure of precise technical features which would render it apparent to the skilled person how to generate the extracted clock signal.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 17-22, 24-26, 29-34, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (U.S. Patent No. 5,745,468) in view of Aoki et al. (U.S. Patent No. 6,236,696 B1).

Regarding claim 17:

As shown in figure 4, Nakano discloses a clock signal extraction device for extracting an extracted clock signal out of a periodic data signals, comprising:

- a first clock generator circuit configured to generate a rising edge clock signal, the first clock generator circuit having a first output (**see figure 4, reference character 3**);

- a first phase detector configured to detect a first phase difference between a rising edge of the periodic data signal and a rising edge of the rising edge clock signal, the first phase detector having a first input connected to the first output to form a first loop, and wherein the first clock generator circuit and the first phase detector cooperate to reduce the detected first phase difference (**see figure 4, reference character 3 where Nakano illustrates a phase-locked loop which is generally built to include a phase detector in order to change the control voltage of the oscillator of the phase-locked loop**);

- a second clock generator circuit configured to generate a falling edge clock signal (**see figure 4, reference character 4**);

- a second phase detector configured to detect a second phase difference between a falling edge of the data signal and a falling edge of the falling edge clock signal, the second phase generator having a second input connected to the second output to form a second loop, and wherein the second clock generator circuit and the second phase detector cooperate to reduce the detected second phase difference (**see figure 4, reference character 4 where Nakano illustrates a phase-locked loop which is generally built to include a phase detector in order to change the control voltage of the oscillator of the phase-locked loop**);

- a third clock generator circuit configured to generate a clock having a phase which is intermediate between those of the first and second clocks (**see figure 4, reference character 12**).

Nakano does not specifically disclose generating the extracted clock signal based on an average of a first phase difference and a second phase difference.

However, Aoki, in the same field of endeavor, discloses generating the extracted clock signal based on an average of a first phase difference and a second phase difference (**see figure 25, reference character 1910**).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the invention of Nakano as taught by Aoki and generate the extracted clock signal based on an average of the first phase difference and the second phase difference such that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged, thus allowing more rapid and accurate data recovery (**Aoki, col. 1, lines 45-50**).

Regarding claim 18:

The combination of Nakano and Aoki discloses the clock signal extraction device according to claim 17, wherein the third clock generator circuit includes a controller and a third clock generator, the controller configured to process said first phase difference and said second phase difference to control generation of the extracted clock signal by the third clock generator (**see Nakano, figure 4, reference character 9a**).

Regarding claim 19:

The combination of Nakano and Aoki discloses the clock signal extraction device according to claim 18, wherein the controller further constitutes a part of the first clock generator circuit and the second clock generator circuit (**see Nakano, figure 4, reference character 9a**).

Regarding claim 20:

The combination of Nakano and Aoki discloses the clock signal extraction device according to claim 19, wherein each of said first, second and third clock generator circuits includes a voltage controlled oscillator (**see Nakano, figure 4, reference characters 3,4, and 12 where Nakano illustrates a phase-locked loop which generally comprises a voltage controlled oscillator**).

Regarding claim 21:

The combination of Nakano and Aoki discloses the clock signal extraction device according to claim 17, wherein each of said first, second and third clock generator circuits includes a voltage controlled oscillator (**e Nakano, figure 4, reference characters 3,4, and 12 where Nakano illustrates a phase-locked loop which generally comprises a voltage controlled oscillator**).

Regarding claim 24:

As shown in figure 4, Nakano discloses an arrangement for extracting data, including: a clock signal extraction device for extracting an extracted clock signal out of a periodic data signal, comprising

- a first clock generator circuit configured to generate a rising edge clock signal, the first clock generator circuit having a first output (**see figure 4, reference character 3**);

- a first phase detector configured to detect a first phase difference between a rising edge of the periodic data signal and a rising edge of the rising edge clock signal, the first phase detector having a first input connected to the first output to form a first loop, and wherein the first clock generator circuit and the first phase detector cooperate to reduce the detected first phase difference (**see figure 4, reference character 3 where Nakano illustrates a phase-locked loop which is generally built to include a phase detector in order to change the control voltage of the oscillator of the phase-locked loop**);

- a second clock generator circuit configured to generate a falling edge clock signal, the second clock generator circuit having a second output (**see figure 4, reference character 4**);

- a second phase detector configured to detect a second phase difference between a falling edge of the data signal and a falling edge of the falling edge clock signal, the second phase generator having a second input connected to the second output to form a second loop, and wherein the second clock generator circuit and the second phase detector cooperate to reduce the detected second phase difference (**see figure 4, reference character 4 where Nakano illustrates a phase-locked loop**

which is generally built to include a phase detector in order to change the control voltage of the oscillator of the phase-locked loop);

- a third clock generator circuit configured to generate a clock having a phase which is intermediate between those of the first and second clocks (**see figure 4, reference character 12**); and
- a data extraction device configured to extract data from said data signal according to a rate of said extracted clock signal (**see figure 4, reference characters 5,6, and 13**).

Nakano does not specifically disclose generating the extracted clock signal based on an average of a first phase difference and a second phase difference.

However, Aoki, in the same field of endeavor, discloses generating the extracted clock signal based on an average of a first phase difference and a second phase difference (**see figure 25, reference character 1910**).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the invention of Nakano as taught by Aoki and generate the extracted clock signal based on an average of the first phase difference and the second phase difference such that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually averaged, thus allowing more rapid and accurate data recovery (**Aoki, col. 1, lines 45-50**).

Regarding claim 25:

The combination of Nakano and Aoki discloses the arrangement according to claim 24, wherein the third clock generator circuit includes a controller and a third clock generator, the controller configured to process said first phase difference and said second phase difference to control generation of the extracted clock signal by the third clock generator (**see Nakano, figure 4, reference character 9a**).

Regarding claim 26:

The combination of Nakano and Aoki discloses the arrangement according to claim 25, wherein said controller controls said third clock generator to generate said Clock signal such that the error rate of the extracted data is minimized (**see Nakano, figure 4, reference character 9a**).

Regarding claim 29:

As shown in figure 4, Nakano discloses a method for extracting an extracted clock signal out of a periodic data signal, comprising:

- (a1) generating a rising edge clock signal (**see figure 4, reference character 3**);
- (a2) detecting a first phase difference between a rising edge of the periodic data signal and a rising edge of a rising edge clock signal (**see figure 4, reference character 3 where Nakano illustrates a phase-locked loop**);
- (a3) feeding back the first phase difference to generate a subsequent rising edge clock signal having a reduced first phase difference (**see figure 4, reference character 3 where Nakano illustrates a phase-locked loop**);

- (b1) generating a falling edge clock signal (**see figure 4, reference character 4**);
- (b2) detecting a second phase difference between a falling edge of the periodic data signal and a falling edge of a falling edge clock signal (**see figure 4, reference character 3 where Nakano illustrates a phase-locked loop**);
- (b3) feeding back the second phase difference to generate a subsequent falling edge clock signal having a reduced second phase difference (**see figure 4, reference character 3 where Nakano illustrates a phase-locked loop**); and
- (c) generating a clock having a phase which is intermediate between those of the first and second clocks (**see figure 4, reference character 12**).

Nakano does not specifically disclose generating the extracted clock signal based on an average of a plurality of first phase differences and second phase differences.

However, Aoki, in the same field of endeavor, discloses generating the extracted clock signal based on an average of a plurality of first phase differences and second phase differences (**see figure 25, reference character 1910**).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the invention of Nakano as taught by Aoki and generate the extracted clock signal based on an average of a plurality of first phase differences and second phase differences in a way that the probability distribution functions of the rising edges and falling edges of the periodic data signal are individually

averaged, thus allowing more rapid and accurate data recovery (**Aoki, col. 1, lines 45-50**).

Regarding claim 30:

The combination of Nakano and Aoki discloses the method according to claim 29, where step (a1) includes employing a voltage controlled oscillator to generate the first clock signal and the subsequent first clock signal (**see Nakano, figure 4, reference characters 3,4, and 12 where Nakano illustrates a phase-locked loop which generally comprises a voltage controlled oscillator**).

Regarding claim 31:

The combination of Nakano and Aoki discloses the method according to claim 30, where step (a2) includes employing a voltage controlled oscillator to generate the second clock signal and the subsequent second clock signal (**see Nakano, figure 4, reference characters 3,4, and 12 where Nakano illustrates a phase-locked loop which generally comprises a voltage controlled oscillator**).

Regarding claim 32:

The combination of Nakano and Aoki discloses the method according to claim 29, further comprising a step of: extracting data from said data signal according to a rate of said extracted clock signal (**see figure 4, reference characters 5,6, and 13**).

Regarding claim 33:

The combination of Nakano and Aoki discloses the method according to claim 32, wherein step c) further comprises generating the extracted clock signal such that the

error rate of said extracted data is minimized **(see Nakano, figure 4, reference character 9a)**.

Regarding claim 34:

The combination of Nakano and Aoki discloses the method according to claim 33, wherein said data signal is an optical data signal **(see Nakano, col. 3, lines 66-67 through col. 4, lines 1-5)**.

Regarding claim 36:

The combination Nakano and Aoki of discloses the method according to claim 29, wherein said data signal is an optical data signal **(see Nakano, col. 3, lines 66-67 through col. 4, lines 1-5)**.

9. Claims 23, 27-28, and 35 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano (U.S. Patent No. 5,745,468) in view of Aoki et al. (U.S. Patent No. 6,236,696 B1) as applied to claims 19, 24, and 33 above, and further in view of Tanji et al. (U.S. Patent No. 6,307,906 B1).

Regarding claim 23:

The combination of Nakano and Aoki discloses the clock signal extraction device according to claim 19.

The combination of Nakano and Aoki does not specifically teach a phase pump and a loop filter.

Tanji discloses a phase pump and a loop filter **(see figure 1, reference characters 20 and 22)**.

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the invention of Nakano and Aoki as taught by Tanji and wherein the controller further comprises, for each of the first, second and third clock generator circuits, a phase pump and a loop filter, thus allowing a reduction in jitter an dchannel crosstalk that can occur with multiple clocks (**Tanji, col. 1, lines 40-45**).

Regarding claim 27:

The combination of Nakano, Aoki, and Tanji discloses the arrangement according to claim 24, wherein said data extraction device comprises a data sampler for sampling said data signal (**see Tanji, figure 1, reference character 14**).

Regarding claim 28:

The combination of Nakano, Aoki, and Tanji discloses the arrangement according to claim 27, wherein said data sampler comprises a D-type flip-flop (**see Tanji, figure 4A**).

Regarding claim 35:

The combination of Nakano, Aoki, and Tanji discloses the method according to claim 33, further comprising extracting data from said data signal using a flip-flop (**see Tanji, figure 4A**).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GINA MCKIE whose telephone number is (571)270-5148. The examiner can normally be reached on Mon-Fri, 9:00 AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Gina McKie/
Examiner, Art Unit 2611
March 17, 2008
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Supervisory Patent Examiner, Art Unit 2611